15.2 A Flexible ISO14443-A Compliant 7.5mW 128b Metal-Oxide NFC Barcode Tag with Direct Clock Division Circuit from 13.56MHz Carrier

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Flexible low-cost RFID/NFC tags have great potential to be embedded in everyday objects providing them a unique identifier or sensor readout facilitating the Internet-of-Everything, whereby a smartphone or tablet is the interface to the Internet-of-Things. The main challenge for flexible metal-oxide RFID tags is to fully comply with the ISO14443-A NFC standard to enable readout by standard NFC reader or handheld devices, due to the limited charge carrier mobility of the semiconductor and multiple sources of parameter variation caused by roughness, temperature and dimensional stability of the foils. Recent work by various groups [1-4] demonstrated only an incremental improvement in data rates from 50b/s to 396.5kb/s to be compatible with ISO14443 (105.9kb/s). In this work, we present a flexible metal-oxide NFC chip that is compliant with ISO14443-A, showcasing advancements on memory size, power consumption and a clock generation circuit.

The flexible self-aligned metal-oxide transistor technology is shown in Fig. 15.2.1. The semiconductor is Indium-Gallium-Zinc-Oxide (IGZO) resulting in n-type thin-film transistors (TFTs) exhibiting a mobility of 13.49cm²/Vs. The cross-section details a scalable self-aligned transistor architecture with channel lengths down to 2 and 1.5µm, and polyimide as flexible substrate. The gate insulator is 100nm SiO_2. 400nm SiN_x serves as decoupling layer between the metallization layers to decrease the parasitic overlap capacitors and acts as doping layer for the semiconductor area, which is not covered by gate dielectric. The local V_T variability of 2µm self-aligned TFTs on flex is 150mV (Fig. 15.2.1).

The ISO14443-A specification describes a bit representation with data rates of 105.9kb/s (13.56MHz carrier divided by 128), Manchester encoding and OOK subcarrier modulation with a clock of 847.5kHz (carrier divided by 16). The logic gate delay to enable clock division is targeted around 10× of the carrier frequency, being 7.37ns. The spec on gate delay is studied by integrating unipolar n-type, pseudo-CMOS inverters [5] into 19-stage ring oscillators. The effect of channel length scaling on the inverter performance is plotted in Fig. 15.2.2, resulting obtained stage delays of 63.4ns for L=5µm and 5.2ns for L=2µm at 5V VDD and 10V VBIAS. In addition, the transistor ratios of the VBIAS branch have been adapted featuring a faster implementation of the pseudo-CMOS inverter (L2F and L1.5F). This reduces the stage delay down to 2.36ns at 5V VDD and 10V VBIAS for the 1.5µm version. Figure 15.2.2 shows that this logic implementation meets the specification for all VDD variations, yielding a more robust division circuit. The clock division circuit is based on negative edge-triggered flipflops. Figure 15.2.2 depicts also the measured clock division range for VDD varying between 3V to 5V. As expected, the 1.5µm fast implementation can divide a 13.56MHz signal over this supply range, with a maximum operating frequency of 27.3MHz.

The drawback of channel length scaling without decreasing the minimum width (10µm) is increased power consumption. The 19-stage ring oscillator (i.e. only 80 n-TFTs) consumes 2.15mW for L=5µm and 30.21mW for L1.5F at 5V VDD and 10V VBIAS, which is the range of incident power of a tag in the NFC field of a smartphone. The power consumption of unipolar pseudo-CMOS logic can mainly be attributed to static leakage paths. Most of the current flows in the VBIAS branch with the largest supply voltage. Four different Low Power (LP) implementations have been realized (LP1-LP4, Fig. 15.2.3) by decreasing the minimal width, targeting more symmetrical currents in both supply branches. These lower currents decrease indeed the power consumption from 15.89mW for L2 to 1.87mW for LP4 at 5V VDD and 10V VBIAS, which is even below the power consumption of L5, as shown in Fig. 15.2.3. However, the power reduction in the LP implementations comes at cost of stage delay.

The preferred standard for the Internet-of-Everything is the Thinfilm NFC Barcode protocol, derived from the ISO14443 Type A NFC standard. It is a tag-talks-first protocol, which transmits 128b code during 1.21ms burst cycles and remains silent for 3.6ms. NFC tags can be detected within 5ms, allowing one to read approximately 200 tags/s. This protocol is supported by the latest NFC controllers embedded in phones and tablets running on Android 4.2 or later. The 128bits is divided into 16 protocol bits, 96 bits of unique ID and 16 bits CRC. The block diagram of the IGZO NFC Barcode chip is shown in Fig. 15.2.4. It comprises a clock generator, a digital core part to read out the 128b ROM and an ISO14443 data formatting block. The clock generator circuit is based on a 7-stage toggle flip-flop divider circuit implemented with different pseudo-CMOS variations. L1.5F is selected as first stage to enable robust operation at 13.56MHz. The last stages are designed by employing the LP3 implementation with 4µm minimal channel length. The same pseudo-CMOS logic variation is used for the digital core generator. It provides two output signals, namely an NRZ-encoded 128b code and an output enable (outEN) to alter between silent or burst mode. The 16 CRC bits are also fully part of the 128b ROM memory, in order to save overall system power by reducing the number of gates. The last block is the data formatting part, which generates the ISO14443-A compatible bit representation from the NRZ encoded input data. It will perform Manchester encoding based on a 212kHz clock and OOK modulation of the 847kHz subcarrier on the high level of the bit sequence. The IGZO NFC Barcode chip starts operating from 3V VDD and 6V VBIAS onwards, consuming only 7.5mW of overall power, shown in Fig. 15.2.4. The NFC Barcode chip employs in total 1712 n-type TFTs and measures 50.55mm². Figure 15.2.7 shows the die micrograph.

Figure 15.2.5 depicts the fully integrated, passive IGZO NFC Barcode tag. It comprises of an HF antenna, a power harvesting circuit (double half-wave rectifier), the IGZO NFC Barcode chip and a load modulation transistor enabling amplitude modulation on the carrier. The reader is an NFC-enabled device. The tag shows correct behavior when applied in the 13.56MHz NFC reader field. The timing of the transmission and silent period is correct, and the 128b transmitted code shows the bit representation as required from ISO14443-A.

The table in Fig. 15.2.6 benchmarks this work to previous IGZO RFID tags. The major achievement of this tag is its compliance to the ISO14443-A NFC Barcode standard, with direct clock division from the 13.56MHz carrier. It embeds a 128b ROM memory. Optimizations at logic gate and system level reduced power consumption down to 7.5mW. These flexible ISO14443-A compliant metal-oxide NFC Barcode tags embedded in everyday objects enable connectivity with a smartphone or tablet as a hub to the Internet-of-Everything.

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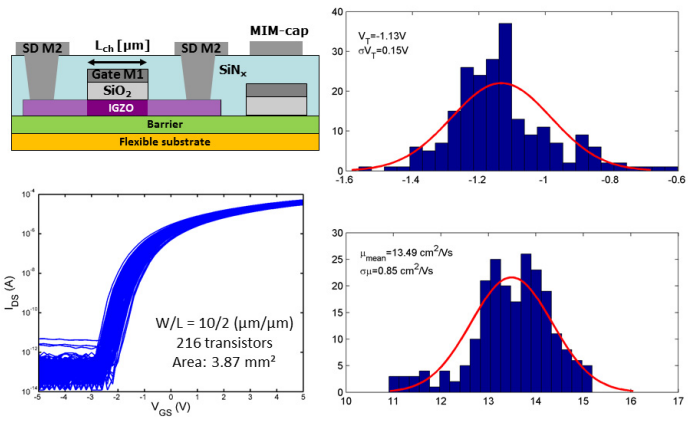

Figure 15.2.1: Device cross-section and TFT transfer curve of scaled self-aligned IGZO TFTs on polyimide foil.

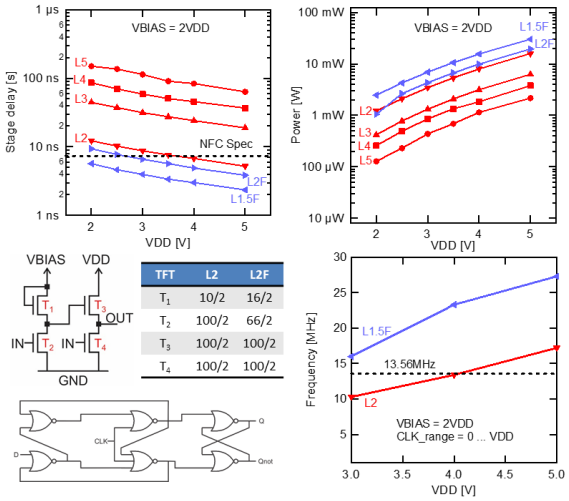

Figure 15.2.2: The impact on stage delay and power of pseudo-CMOS inverters with scaled technology, from L= 5µm to L = 2µm (L5-L2) and for two fast implementations of pseudo-CMOS inverters (L2F and L1.5F).

TFT	LP1	LP2	LP3	LP4
T_1	4/2	4/2	4/4	2/4
T_2	40/2	40/2	20/2	10/2
T_3	100/2	60/2	60/2	60/2
T_4	100/2	60/2	60/2	60/2

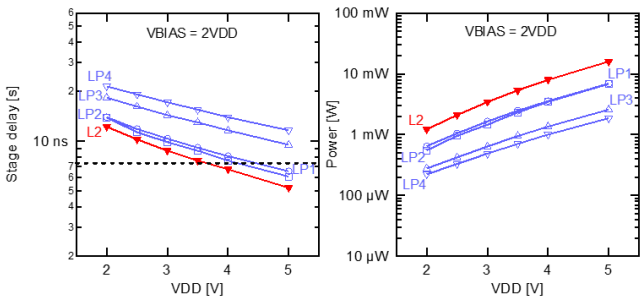

Figure 15.2.3: Overview of 4 different low power implementations (LP1-LP4) in case of pseudo-CMOS logic and direct comparison of measured stage delay and power versus its supply voltage for the low power implementations with respect to the regular L2 implementation.

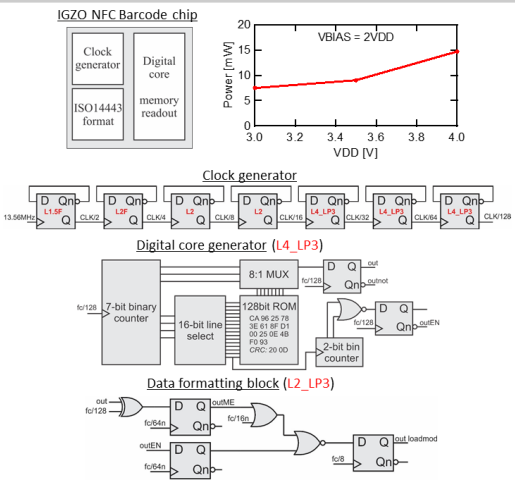

Figure 15.2.4: IGZO NFC Barcode chip block diagram and its measured power consumption as a function of supply voltage. The lower part details the circuit implementation of the clock generator, the digital core generator (channel length 4, LP3) and the data formatting block (channel length 2, LP3).

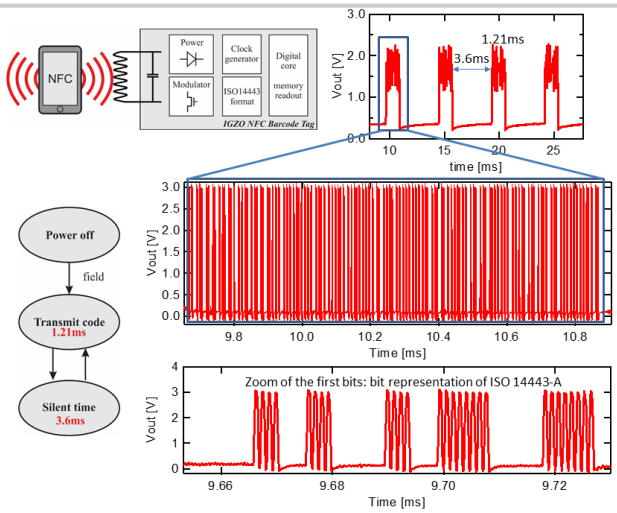

Figure 15.2.5: Measurement details of the fully integrated IGZO NFC barcode tag displaying correct behavior when approached with an NFC reader device. The fully integrated block diagram is indicated at the top left.

	[This work] Pseudo CMOS SAL	[4] Pseudo CMOS SAL	[3] Pseudo CMOS	[3] Dual-gate M2	[3] Dual-gate M3	[3] Diode-load	[1] Zero-V_{GS} load	[2] Diode-load
# TFTs/inv	4	4	4	2	2	2	2	2
Footprint inverter [µm²]	29277	36425	65812	40300	19350	19350	n.a.	n.a.
Chip area [mm²]	6.03x8.38 (50.55)	3.42x3.19 (10.884)	4.69x3.36 (15.759)	3.91x3.87 (15.132)	2.70x3.14 (8.478)	2.70x2.98 (8.046)	7x10 (70)	3.9x1.5 (5.85)
# TFTs	1712	438	436	218	218	218	1026	222
# supplies	3	3	3	3	3	2	2	2
Memory	128-bit (96-bit unique)	12-bit	12-bit	12-bit	12-bit	12-bit	Preamble + 4-bit ROM	16-bit
Stage delay ring osc	2.4ns	63.0ns	569.5ns	2.2µs	969.0ns	349.2ns	909.1µs	7.8µs
Clock generation	Division from carrier	19-stage ring osc	19-stage ring osc	19-stage ring osc	19-stage ring osc	19-stage ring osc	11-stage ring osc	9-stage ring osc
Data rate	105.9kbit/s $f_c/128$	396.5kbit/s	43.9kbit/s	11.3kbit/s	25.8kbit/s	71.6kbit/s	0.05kbit/s	3.2kbit/s
Subcarrier frequency	847.5kHz $f_c/16$	None	None	None	None	None	None	None
ISO compliant	ISO14443-A NFC Barcode	No	No	No	No	No	No	No
Reader	Smartphone and tablet	Custom reader	Custom reader	Custom reader	Custom reader	Custom reader	Custom reader	Custom reader
Software	Android 4.2 onwards	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.
Substrate	PI-foil	PI-foil	PEN-foil	PEN-foil	PEN-foil	PEN-foil	Glass	Glass

Figure 15.2.6: Summary and comparison to state of the art.

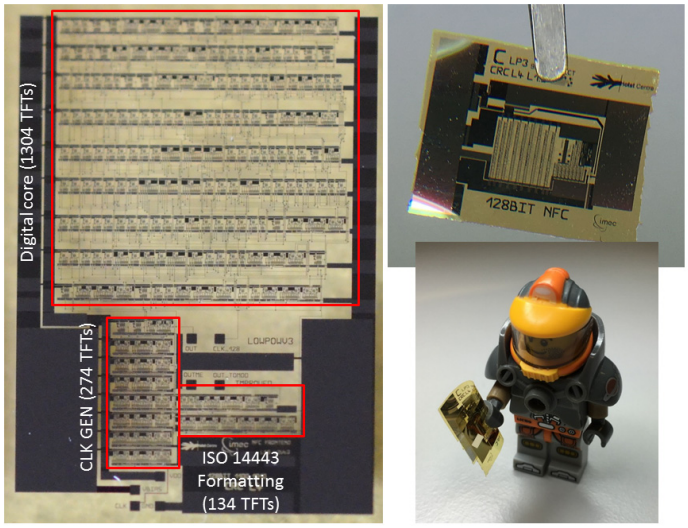

Figure 15.2.7: (left) Die micrograph of the IGZO NFC Barcode foil and (right) photograph of the flexible integrated NFC Barcode (without antenna).

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